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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,773	02/26/2002	Robert Bruce Ganton	UTL 00080	1999

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,773	GANTON, ROBERT BRUCE	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on August 09, 2004. This amendment has been entered and carefully considered. Claims 1-10 and 12-43 are cancelled; and claims 44-63 are newly added for examination.

2. The objection to claims 34-38 cited in the previous office action is now moot since these claims are cancelled due to the Amendment filed on August 09, 2004.

3. Applicant's arguments filed on August 09, 2004 have been fully considered but they are not deemed to be persuasive.

4. Applicant's arguments filed on August 09, 2003 have been fully considered but deemed to be moot in view of new ground rule rejection.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the communication circuit that comprises a transmitter circuit, a receiver circuit, and an antenna; and connected to and controlled by the processing unit" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 44-48, 50-58, 60-61 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (USPN: 2003/0050087) in view of Lofgren et al. (USPN: 2002/0032843) hereinafter, Lofgren.

As per claims 44, Kwon teaches a wireless communications device, comprising:

- a non-volatile memory for storing data (NAND-type flash memory 210 in Fig. 2A);

- a processing unit (microprocessor 220 in Fig. 2A) comprising:
  - a read-only memory (ROM of ASIC 215 in Fig. 2A) comprising code (boot code) for providing instructions for reading the data from the non-volatile memory (NAND-type flash memory 210 in Fig. 2A) (e.g. see paragraph 31 on page 3);
- a volatile addressable memory (first and second RAM 230, 235 in Fig. 2A) for storing at least a portion of the data stored in the non-volatile memory, the volatile addressable memory connected to the processing unit (MPU 220 in Fig. 2A) by parallel address (224 thru 215 in Fig. 2A) and data lines (222 in Fig. 2A);
- a communications circuit (analog circuit 240 in Fig. 2A) connected to and controlled by the processing unit, the communications circuit comprising:
  - a transmitter circuit (embedded in 240 of Fig. 2A);
  - a receiver circuit (embedded in 240 of Fig. 2A); and
  - an antenna (ANT in Fig. 2A) connected to the transmitter circuit and the receiver circuit (e.g. see paragraphs 24-26 on page 2).

However, Kwon does not teach that the processing unit comprises the ROM, i.e. ROM is a part of the processing unit. However, it is very well known in the art that by fabricating the multiple components on the same chip can reduce the data latency and therefore increases the overall performance of the system. The Examiner herein taking Official Notice on this subject matter.

Furthermore, Kwon does not teach that the processing unit comprises a serial interface controller. Lofgren, on the other hand, teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 56, Kwon teaches a method for managing a wireless communications device, comprising the steps of:

- executing instructions from a read-only memory (ROM of ASIC 215 in Fig. 2A) in a processing unit (microprocessor 220 in Fig. 2A); and
- transferring the parallel data (i.e. data and address in parallel) to a volatile memory (RAM1 and RAM2, 230 and 235 in Fig. 2A) over parallel address and data lines (222 and 224 in Fig. 2A).

Furthermore, Kwon discloses that the program stored in the non-volatile memory (the NAND-type flash memory) gets copied into the volatile addressable memory (the RAM1) to execute that program by the RAM2 (e.g. see paragraph 25 on page 2). The volatile memory (RAM1 and RAM2) of the wireless communications device (the mobile

phone) taught by Kwon is smaller in size compare to the non-volatile memory (the NAND-type flash memory). Therefore, when the interface controller (the MPU) requests the data stored in the indirectly-read memory, the device has to transfer only a portion of the data stored in the non-volatile memory to the addressable volatile memory due to the limited space and if the interface controller requests the another data, which is currently not stored in the addressable volatile memory, the memory interface will transfer that data to the addressable volatile memory for further processing, i.e. the operation of the communications circuit of the wireless communications device in response to the at least a portion of the transferred data gets started.

The further limitation of converting the serial data to parallel data is well-known and notorious old in the art. The examiner herein taking Official Notice on this subject matter.

Although, Kwon teaches the method comprising a parallel interface controller (215 in Fig. 2A) to read the parallel data from the non-volatile memory (e.g. see Fig. 2A), Kwon does not teach that the method comprises a serial interface controller to read the serial data from the non-volatile memory over a serial address and data line. Lofgren, on the other hand, teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without

hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 61, Kwon teaches a wireless communications device, comprising:

- a wireless communications circuit (analog circuit 240 in Fig. 2A) comprising;
    - o a receiver (embedded in 240 of Fig. 2A);
    - o a transmitter (embedded in 240 of Fig. 2A); and
    - o an antenna (ANT in Fig. 2A) connected to the receiver and the transmitter;
- a volatile memory (first and second RAM 230, 235 in Fig. 2A); and
- a processor (microprocessor 220 in Fig. 2A) connected to the wireless communications circuit, the processor comprising:
    - o a read only memory (ROM of ASIC 215 in Fig. 2A) for storing read instructions;
    - o a serial interface connected to the volatile memory (RAM1 and RAM2, 230 and 235 in Fig. 2A) by parallel address and data lines (222 and 224 in Fig. 2A); and
    - o wherein the processor controls the wireless communications circuit based upon the stored parallel data in the volatile memory (e.g. see paragraph 31 on page 3).

However, Kwon does not teach that the processing unit comprises the ROM, i.e. ROM is a part of the processing unit. However, it is very well known in the art that by

fabricating the multiple components on the same chip can reduce the data latency and therefore increases the overall performance of the system. The Examiner herein taking Official Notice on this subject matter.

The further limitation of converting the serial data to parallel data is well-known and notorious old in the art. The examiner herein taking Official Notice on this subject matter.

Although, Kwon teaches the method comprising a parallel interface controller (215 in Fig. 2A) to read the parallel data from the non-volatile memory during boot-up (e.g. see Fig. 2A), Kwon does not teach that the method comprises a serial interface controller to read the serial data from the non-volatile memory over a serial address and data line during boot up condition. Lofgren, on the other hand, teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

As per claims 45-47, 57-58 and 63, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the

wireless communications device, wherein the flash (non-volatile) memory can be a NAND-type flash memory (which is referred as serial flash memory in the 'Background of the Invention' section of this application) or a NOR-type flash memory (which is referred as parallel flash memory in the 'Background of the Invention' section of this application) (e.g. see paragraph 26 on page 2). Accordingly, either the clocked parallel flash memory or the clocked serial flash memory can be used as the non-volatile memory; based on this rationale, claims 45-47, 57-58 and 63 are rejected.

As per claim 48, the combination of Kwon and Lofgren teaches the wireless communications device, which uses the NAND-type flash memory. The NAND-type flash memory is one of the non-volatile memory type being implemented in Kwon's system; in addition, neither Applicant's specification nor the claimed invention disclose that different type of non-volatile memories would yield different function of the system operation. Therefore, any type of non-volatile memories including the indexed addressable memory and the addressable, serially interfaced memory can be used in the place of NAND-type flash memory.

As per claims 50-51 and 60, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the wireless communications device, wherein the addressable volatile memory (RAM1 and RAM2 230, 235 in Fig. 2A) is a Random Access Memory (RAM) (e.g. see lines 8-9 of paragraph 25); in addition, neither Applicant's specification nor the claimed invention disclose that different type of volatile memories would yield different function of the system operation. Therefore, any type of volatile memories including the dynamic

random access memory (DRAM) and the static random access memory (SRAM), can be used. Kwon also teaches that the wireless communications device uses the NAND-type flash memory. The NAND-type flash memory (which is referred as indirectly-read memory in the 'Background of the Invention' section of this application) is one of the non-volatile memory being implemented in Kwon's system; in addition, neither Applicant's specification nor the claimed invention disclose that different type of non-volatile memories would yield different function of the system operation. Therefore, any type of non-volatile memories including Multimedia Card, Smart Media Card, SD Card, and Memory Stick, can be used in place of the NAND-type flash memory.

As per claim 52, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches that the code of the read only memory (ROM of ASIC 215 in Fig. 2A) comprises a first code (the boot code) section for determining whether the non-volatile memory is connected to the serial memory interface controller (i.e. connection of the flash memory is checked by checking the contents of the flash memory in the step 304 of the flow diagram shown in the Fig. 3). Furthermore, Kwon discloses that the program stored in the non-volatile memory (the NAND-type flash memory) gets copied into the volatile addressable memory (the RAM1) to execute that program by the RAM2 (e.g. see paragraph 25 on page 2). The volatile memory (RAM1 and RAM2) of the wireless communications device (the mobile phone) taught by Kwon is smaller in size compare to the non-volatile memory (the NAND-type flash memory). Therefore, when the interface controller (the MPU) requests the data stored in the indirectly-read memory, the device has to transfer only a portion

of the data stored in the non-volatile memory to the addressable volatile memory due to the limited space and if the interface controller requests the another data, which is currently not stored in the addressable volatile memory, the memory interface will transfer that data to the addressable volatile memory for further processing.

As per claims 53-55, the combination of Kwon and Lofgren discloses the claimed invention as described above, and furthermore, Kwon teaches the wireless communications device comprising the NAND-type flash memory which stores all application programs as well as other types of user data (e.g. see lines 3-7 of paragraph 25). Some of these application programs, for example, an operating system and calibration parameters, are critical to the operation of the wireless communications device; and some of these application programs, for example, interface information, a recent call list, display settings, roaming preferences, ringer preferences and a phone book, are not critical to the operation of the wireless communications device. Based on this rationale, claims 53-55 are rejected.

7. Claims 49, 59 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Lofgren, further in view of Christensen et al. (EP 1 189 465 A1), hereinafter, Christensen.

As per claims 49, 59 and 62, the combination of Kwon and Lofgren discloses the claimed invention as described above. However, both Kwon and Lofgren failed to teach that the non-volatile memory is removably connected to the serial memory interface controller. Christensen, on the other hand, teaches the memory module (5 in Fig. 1) is

removably connected to the terminal control means (2 in Fig. 1) by an interface (4 in Fig. 1) having several connections for exchanging information between the terminal control means and the memory control means (6 in Fig. 1) (e.g. see the abstract and Fig. 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the method and device taught by the combination of Kwon and Lofgren by removably connecting the non-volatile memory to the interface controller as taught by Christensen. In doing so, the removable memory advantageously combines an extended memory function and a subscriber identity module function. Therefore, it is being advantageous.

Remarks

8. As to the remark, Applicant asserted that

(a) With regards to independent claims 44, 56 and 61, there is no motivation or suggestion to combine the Kwon and Lofgren references in such a manner as to make the independent claims 44, 56 and 61 obvious as it required by the first *prima facie* requirement.

(b) Referring to Figures IB and 7B and paragraph 90 of the Lofgren reference, the controller module 133 of Lofgren would be inoperable if placed in a Kwon device since "some of the controller module's functions are performed by the system microprocessor 121 and other system resources of the computer system 101."

of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated above in the rejection of claims 44, 56 and 61, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required.

With respect to (b), paragraph 90 of Lofgren states, "Unlike the control module 133 of Fig. 7A, some of the controller module's functions are performed by the system microprocessor 121 and other system resources of the computer system 101 (see Fig. 1B)", i.e. the control module 133 of Fig. 7A is different from the control module of Fig. 1B.

With respect to (c), Kwon clearly teaches that "The ROM of the ASIC 215 stores program codes for downloading application codes, managing files of the NAND-type flash memory, reading the application program and font data from the NAND-type flash memory and copying them in the RAM, and jumping to a starting address of the RAM" (e.g. see Kwon, paragraph 26).

With respect to (d) and (e), Examiner agrees with Applicant that Kwon does not teach or suggest the use of the serial interface controller and reading serial data from the non-volatile memory as claimed. However, as stated above, Lofgren, on the other hand, teaches that by having a serial interface (to read data serially from the non-volatile memory), a controller can be designed to support memory devices of differing

(c) The addition of ROM to the processor to initiate transfer of data from the mass storage to the RAM as claimed by Applicant, is neither taught nor suggested by the Kwon and Lofgren references.

(d) With regards to claims 44-55, Kwon does not teach or suggest the use of the serial interface controller as claimed.

(e) With regards to claims 56-60, Kwon does not teach or suggest reading serial data from the non-volatile memory.

(f) With regards to claims 56-60, Lofgren does not teach or suggest executing instruction from a ROM in a processing unit to direct a serial interface to read non-volatile memory.

(g) With regards to claims 61-63, Lofgren does not teach or suggest a processor connected to wireless communications circuit.

(h) The statement by Examiner, "However, it seems like the use of serial interface is referred to only clocked serial memory and not the clocked parallel memory because the clocked parallel memory has to use some type of parallel interface" (in the previous Office Action), is unsupported by a reference.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one

capacities without modifications to the system (e.g. see page 4, paragraph 60). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's teaching. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous.

With respect to (f), as described above in the response to argument (c), Kwon teaches executing instruction from a ROM in a processing unit to read non-volatile memory. As described above in the response to arguments (d) and (e), Lofgren teaches the use of serial interface in place of parallel interface. Accordingly, the combination of Kwon and Lofgren teaches the limitation of executing instruction from a ROM in a processing unit to direct a serial interface to read non-volatile memory since the parallel interface is replaced by the serial interface by combining the teachings of Kwon and Lofgren.

With respect to (g), both Kwon and Lofgren teach that a processor connected to wireless communications circuit (e.g. 417 in Fig. 7A of Lofgren; 220 in Fig. 2A of Kwon).

With respect to (h), Applicant defines "indirectly-read memory" as "clocked serial memory, clocked parallel memory, indexed addressable memory, and addressable devices that use some from of serial interface" on page 7, second paragraph. Examiner asserted the statement "However, it seems like the use of serial interface is referred to

only clocked serial memory and not the clocked parallel memory because the clocked parallel memory has to use some type of parallel interface" because it is in the knowledge generally available to one of ordinary skill in the art that the serial memory uses the serial interface and not the parallel memory.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ross (USPN: 6,400,725) teaches the benefits of using serial interface in place of parallel interface (e.g. see Col. 1, lines 11-28).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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